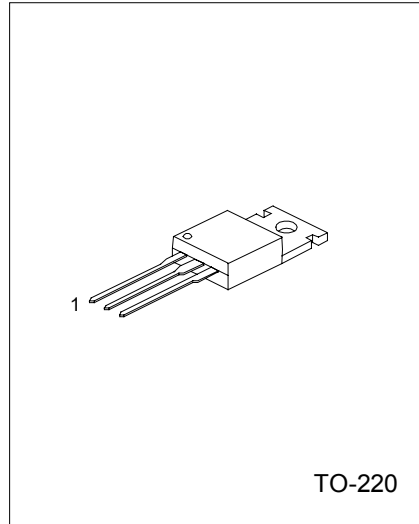
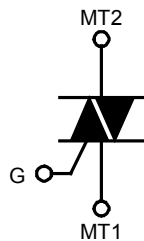


TRIACS

DESCRIPTION

Passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

SYMBOL



1:MT1 2:MT2 3:GATE

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Repetitive Peak Off-State Voltage UT137E-5 UT137E-6 UT137E-8	V <sub>DRM</sub>	500* 600* 800	V
RMS On-state Current Full sine wave; T <sub>mb</sub> ≤ 102°C	I <sub>T(RMS)</sub>	8	A
Non-Repetitive Peak. On-State Current Full sine wave; T <sub>j</sub> = 25°C prior to surge t = 20ms t = 16.7ms	I <sub>TSM</sub>	65 71	A
I <sup>2</sup> t For Fusing (t = 10ms)	I <sup>2</sup> t	21	A <sup>2</sup> s
Repetitive Rate of Rise of On-state Current after Triggering I <sub>TM</sub> = 12A; I <sub>G</sub> = 0.2A, dI <sub>G</sub> /dt = 0.2A/μs T2+ G+ T2+ G- T2- G- T2- G+	dI <sub>T</sub> /dt	50 50 50 10	A/μs
Peak Gate Voltage	V <sub>GM</sub>	5	V
Peak Gate Current	I <sub>GM</sub>	2	A
Peak Gate Power	P <sub>GM</sub>	5	W
Average Gate Power (Over any 20ms period)	P <sub>G(AV)</sub>	0.5	W
Operating Junction Temperature	T <sub>J</sub>	125	°C
Storage Temperature	T <sub>stg</sub>	-40~150	°C

\*Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6A/μs.

## THERMAL RESISTANCES

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Thermal Resistance Junction to Mounting Base Full cycle Half cycle	Rth j-mb			2.0 2.4	K/W
Thermal Resistance Junction to Ambient In free air	Rth j-a		60		K/W

STATIC CHARACTERISTICS (T<sub>j</sub>=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gate Trigger Current	I <sub>GT</sub>	V <sub>D</sub> =12V, I <sub>T</sub> =0.1A T2+ G+ T2+ G- T2- G- T2- G+		2.5 4.0 5.0 11	10 10 10 25	mA
Latching Current	I <sub>L</sub>	V <sub>D</sub> =12V, I <sub>GT</sub> =0.1A T2+ G+ T2+ G- T2- G- T2- G+		3.0 14 3.0 4.0	25 35 25 35	mA
Holding Current	I <sub>H</sub>	V <sub>D</sub> =12V, I <sub>GT</sub> =0.1A		2.5	20	mA
On-State Voltage	V <sub>T</sub>	I <sub>T</sub> =10A		1.3	1.65	V
Gate Trigger Voltage	V <sub>GT</sub>	V <sub>D</sub> =12V, I <sub>T</sub> =0.1A V <sub>D</sub> =400V, I <sub>T</sub> =0.1A, T <sub>j</sub> =125°C	0.25	0.7 0.4	1.5	V
Off-state Leakage Current	I <sub>D</sub>	V <sub>D</sub> =V <sub>DRM(max)</sub> , T <sub>j</sub> =125°C		0.1	0.5	mA

DYNAMIC CHARACTERISTICS (T<sub>j</sub>=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Critical Rate of Rise of off-state Voltage	dV <sub>D</sub> /dt	V <sub>DM</sub> =67% V <sub>DRM(max)</sub> , T <sub>j</sub> =125°C Exponential waveform, Gate open circuit		50		V/μs
Gate Controlled Turn-on Time	t <sub>gt</sub>	I <sub>TM</sub> =12A, V <sub>D</sub> =V <sub>DRM(max)</sub> , I <sub>G</sub> =0.1A dI <sub>G</sub> /dt=5A/μs		2		μs

TYPICAL CHARACTERISTICS

Figure 1. Maximum on-state Dissipation.  $P_{tot}$  vs RMS On-state Current,  $I_T(RMS)$ , Where  $\alpha$  = conduction Angle.

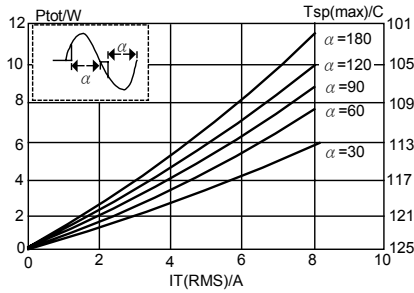


Figure 4. Maximum Permissible RMS Current  $I_T(RMS)$  vs mounting base Temperature  $T_{mb}$

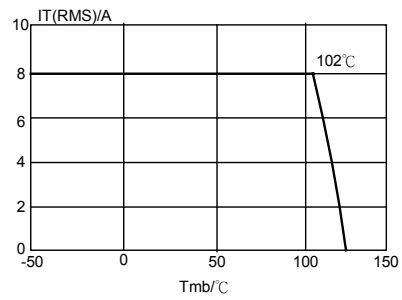


Figure 2. Maximum Permissible Non-repetitive Peak On-state Current  $I_{TSM}$ , vs Pulse Width  $t_p$ , for Sinusoidal Currents,  $t_p \leq 20ms$

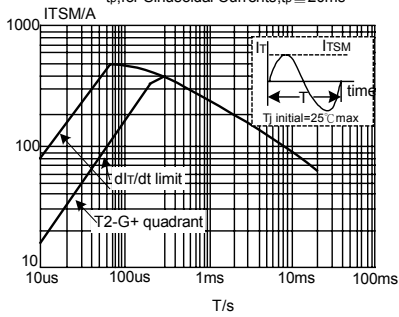


Figure 5. Maximum Permissible Repetitive RMS on-state Current  $I_T(RMS)$ , vs Surge Duration, for Sinusoidal Currents,  $f=50Hz$ ;  $T_{mb} \leq 102^\circ C$

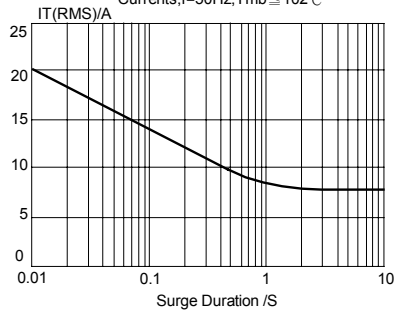


Figure 3. Maximum Permissible Non-Repetitive peak on-state Current  $I_{TSM}$ , vs Number of Cycles, for Sinusoidal Currents,  $f=50Hz$

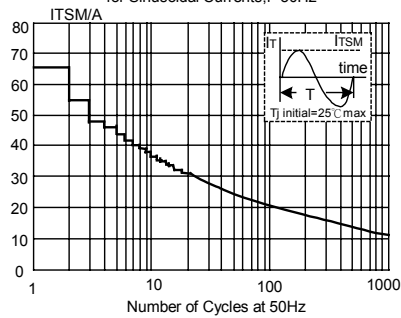


Figure 6. Normalised Gate Trigger Voltage  $V_{GT}(T_j) / V_{GT}(25^\circ C)$ , vs Junction Temperature  $T_j$

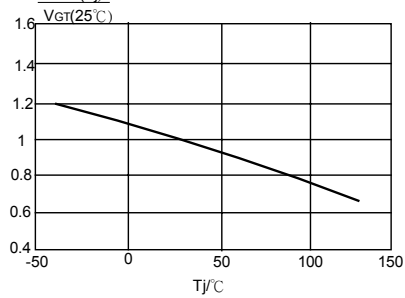


Figure 7. Normalised Gate Trigger Current  $I_{GT}(T_j)/I_{GT}(25^\circ\text{C})$ , vs Junction Temperature  $T_j$

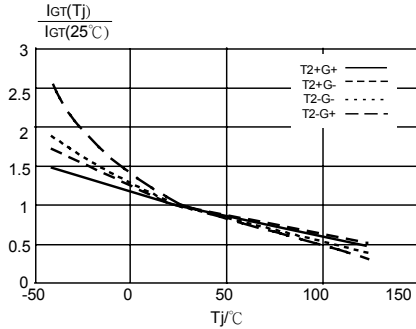


Figure 8. Normalised Latching Current  $I_L(T_j)/I_L(25^\circ\text{C})$ , vs Junction Temperature  $T_j$

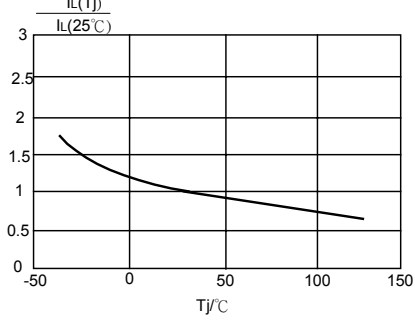


Figure 9. Normalised Holding Current  $I_H(T_j)/I_H(25^\circ\text{C})$ , vs Junction Temperature  $T_j$

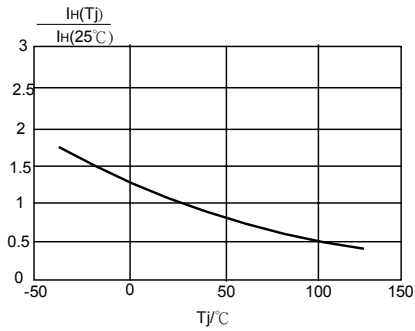


Figure 10. Typical and Maximum On-state Characteristic

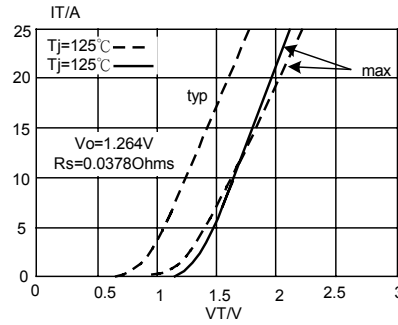


Figure 11. Transient Thermal Impedance  $Z_{th j-mb}$ , vs Pulse Width  $t_p$

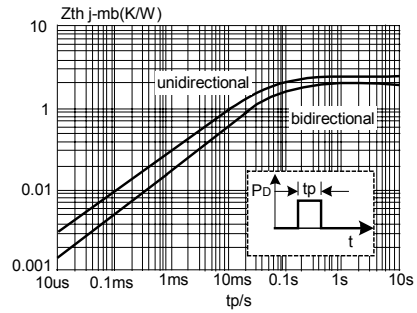
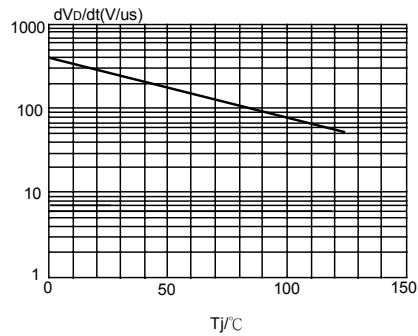


Figure 12. Typical, critical rate of rise of off-state voltage,  $dV_D/dt$  versus junction temperature  $T_j$



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